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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,667	04/23/2001	Kazuhiro Yamada	NAK1-BO60	4146

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2675	9

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/840,667	YAMADA ET AL.	
	Examiner	Art Unit	
	Uchendu O Anyaso	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-12,16,17,23 and 28* is/are allowed.

6)☒ Claim(s) *1-4, 13-15, 18-22, 24-27 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. **Claims 1-29** are pending in this action.

Claim Rejections - 35 USC ' 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 3, 4, 13, 18, 19, 21, 22, 24, 26, 27** and **29** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Awamoto* (U.S. 5,898,414) in view of *Naka et al* (U.S. 6,407,506).

Regarding **independent claims 3, 18** and **19**, Awamoto teaches a PDP image display including a panel having a first electrode which extends in a first direction to write image data and a second electrode which extends in a second direction to select a display line (figure 7 at 1, 2, 5), wherein a field period is divided into a plurality of subfields that each have a predetermined luminance weight, and a grayscale image for the field period is displayed by writing subfield image data of each subfield period obtained by dividing input image data of the field period into the plurality of subfield periods, into the panel through first electrode and the second electrode (column 1, lines 33-38) and sustaining an illumination state of on and off in each cell for each subfield period using luminance equivalent to a luminance weight of each subfield period based on the written sub-field image data (column 1, lines 27-38).

Furthermore, Awamoto teaches conditions and effects to the PDP when the display data gets shorter or when the display data gets longer (column 9, lines 33-45) in order to reduce flicker.

Furthermore, Awamoto teaches how a subfield period are uniformly ON by teaching a display control circuit that varies a light producing period during each of j subframes such that the display control circuit controls a total light producing period within one frame so that the total light producing period remains constant (column 2, lines 36-41).

However, Awamoto does not teach an image changing part. On the other hand, Naka teaches an image changing part by teaching data thinning in a PDP device wherein a technique for a displaying an image by illuminating pixels of a display unit such that data thinning shortens address periods but wherein light emission amounts of the subfields are made identical (column 1, lines 5-8; column 10, lines 21-35, figure 8).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Awamoto and Naka because while Awamoto teaches how a display control circuit that varies a light producing period during each of j subframes such that the display control circuit controls a total light producing period within one frame so that the total light producing period remains constant (column 2, lines 36-41), Naka teaches an image changing part by teaching data thinning in a PDP device wherein a technique for a displaying an image by illuminating pixels of a display unit such that data thinning shortens address periods but wherein light emission amounts of the subfields are made identical (column 1, lines 5-8; column 10, lines 21-35, figure 8). The motivation for combining these inventions would have been to produce a high resolution, finely grade image in a plasma display device (column 2, lines 60-63).

Regarding **claims 4** and **13**, and for **claims 24** and **29**, Awamoto teaches a PDP image display including a panel having a first electrode which extends in a first direction to write image data and a second electrode which extends in a second direction to select a display line (figure 7 at 1, 2, 5), wherein a field period is divided into a plurality of subfields that each have a predetermined luminance weight, and a grayscale image for the field period is displayed by writing subfield image data of each subfield period obtained by dividing input image data of the field period into the plurality of subfield periods, into the panel through first electrode and the second electrode (column 1, lines 33-38) and sustaining an illumination state of on and off in each cell for each subfield period using luminance equivalent to a luminance weight of each subfield period based on the written sub-field image data (column 1, lines 27-38).

Furthermore, Awamoto teaches how the frame cycle for input display data gets shorter, that is, when the frame frequency increases, control is given automatically so that the number of low-order subframes during which interlaced-scanning display is carried out increases such that a display operation can therefore be carried out without any decrease in the number of subframes. Also, by contrast, when the frame cycle for input display data gets longer, that is, when the frame frequency decreases, control is given automatically so that the number of low-order subframes during which interlaced-scanning display is carried out decreases (column 9, lines 25-43, figure 9).

Furthermore, the display control circuit varies a light producing period during each of j subframes such that the display control circuit controls a total light producing period within one frame so that the total light producing period remains constant (column 2, lines 36-41).

However, Awamoto does not teach an image changing part. On the other hand, Naka teaches an image changing part by teaching data thinning in a PDP device wherein a technique for a displaying an image by illuminating pixels of a display unit such that data thinning shortens address periods but wherein light emission amounts of the subfields are made identical (column 1, lines 5-8; column 10, lines 21-35, figure 8).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Awamoto and Naka because while Awamoto teaches how a display control circuit that varies a light producing period during each of j subframes such that the display control circuit controls a total light producing period within one frame so that the total light producing period remains constant (column 2, lines 36-41), Naka teaches an image changing part by teaching data thinning in a PDP device wherein a technique for a displaying an image by illuminating pixels of a display unit such that data thinning shortens address periods but wherein light emission amounts of the subfields are made identical (column 1, lines 5-8; column 10, lines 21-35, figure 8). The motivation for combining these inventions would have been to produce a high resolution, finely grade image in a plasma display device (column 2, lines 60-63).

Regarding **claims 21, 22, 26** and **27**, in further discussion of claims 3 and 4, Awamoto does not teach an image changing unit that changes a part of the subfield image data only when the predetermined subfield period has a smaller luminance weight. On the other hand, Naka teaches an image changing part by teaching data thinning in a PDP device wherein a technique for a displaying an image by illuminating pixels of a display unit such that data thinning

shortens address periods but wherein light emission amounts of the subfields are made identical (column 1, lines 5-8; column 10, lines 21-35, figure 8).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Awamoto and Naka because while Awamoto teaches how a display control circuit that varies a light producing period during each of j subframes such that the display control circuit controls a total light producing period within one frame so that the total light producing period remains constant (column 2, lines 36-41), Naka teaches an image changing part by teaching data thinning in a PDP device wherein a technique for a displaying an image by illuminating pixels of a display unit such that data thinning shortens address periods but wherein light emission amounts of the subfields are made identical (column 1, lines 5-8; column 10, lines 21-35, figure 8). The motivation for combining these inventions would have been to produce a high resolution, finely grade image in a plasma display device (column 2, lines 60-63).

4. **Claims 1, 2, 14, 15, 20** and **25** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Awamoto* (U.S. 5,898,414) in view of *Tajima* (EP 0945844).

Regarding **claims 1** and **2**, Awamoto a PDP image display including a panel having a first electrode which extends in a first direction to write image data and a second electrode which extends in a second direction to select a display line (figure 7 at 1, 2, 5), wherein a field period is divided into a plurality of subfields that each have a predetermined luminance weight, and a grayscale image for the field period is displayed by writing subfield image data of each subfield period obtained by dividing input image data of the field period into the plurality of subfield periods, into the panel through first electrode and the second electrode (column 1, lines

33-38) and sustaining an illumination state of on and off in each cell for each subfield period using luminance equivalent to a luminance weight of each subfield period based on the written sub-field image data (column 1, lines 27-38).

However, Awamoto does not teach an image changing unit that changes a part of the subfield image data so that a total number of charges and discharges performed on a first electrode when writing becomes smaller. On the other hand, Tajima teaches this concept of achieving smaller charges and discharges by teaching a method of driving displays comprising a sequence changing unit for changing a sequence of scanning electrodes to minimize power consumption associated with charging and discharging the electrodes (column 2, lines 23-31; column 1, lines 3-28, 35-40).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Awamoto and Tajima's inventions because while Awamoto teaches how a PDP image display sustains an illumination state of on and off in each cell for each subfield period using luminance equivalent to a luminance weight of each subfield period based on the written sub-field image data (column 1, lines 27-38), Tajima teaches a means for minimizing power consumption by a sequence changing unit for changing a sequence of scanning electrodes such that the charging and discharging performed on the electrode is minimized (column 2, lines 23-31; column 1, lines 3-28, 35-40). The motivation for combining these invention would have been to minimize power consumption on the display device without deteriorating the quality of displayed images (column 1, lines 50-53).

Regarding **claims 14, 15, 20** and **25**, in further discussion of claims 1 and 2, Tajima teaches how to achieve smaller charges and discharges by teaching a method of driving displays comprising a sequence changing unit for changing a sequence of scanning electrodes to minimize power consumption associated with charging and discharging the electrodes (column 2, lines 23-31; column 1, lines 3-28, 35-40).

Allowable Subject Matter

5. **Independent claim 5,** and dependent **claims 6-12, 23** and **28** are allowed.

None of the references, either singularly or in combination, teach or fairly suggest an image display device wherein the cells corresponding to the pixels which form the part of the subfield image data are uniformly one of ON and OFF in the predetermined subfield period, if the luminance weight of the predetermined subfield period is the **smallest** weight.

6. **Claims 16** and **17** allowed.

Response to Arguments

7. Applicant's arguments with respect to claims 3, 4, 13, 18, 19, 21, 22, 24, 26, 27 and 29 filed March 1, 2004 have been fully considered but they are moot in view of the new grounds for rejections.

8. Applicant's arguments with respect to claims 1, 2, 14, 15, 20 and 25 have been considered but they are not persuasive.

With respect to these claims, applicant argues that the Tajima reference performs selective scanning instead of sequential scanning. Furthermore, applicant contends that his invention sequentially scans the display electrode lines from top to bottom on the screen, to write the sub-field image. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., sequential scanning) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

As such, the arguments related to these claims are not persuasive.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Uchendu O. Anyaso whose telephone number is (703) 306-5934. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached at (703) 305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, 6th Floor (Receptionist). Any inquiry of a general nature or relating to the status of this

application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Uchendu O. Anyaso

05/28/2004

CHANH NGUYEN
PRIMARY EXAMINER